What Is Claimed Is:

1. An apparatus, comprising:

N bus lines, wherein N is a natural number;

$\log_2(N)$ pairs of bit lines, wherein each of said $\log_2(N)$ pairs of bit lines includes a high bit line and a low bit line, and wherein each of said N bus lines is coupled to one of said high and low bit lines;

$\log_2(N)$ NOR gates, each having at least a first input, a second input and an output, wherein each NOR gate is associated with one of said $\log_2(N)$ pairs of bit lines, and wherein for each NOR gate, said first input is coupled to said high bit line and said second input is coupled to said low bit line of one of said $\log_2(N)$ pairs; and

a multi-hit line coupled to each output of said $\log_2(N)$ NOR gates.

2. The apparatus of claim 1, wherein N is a positive number.

3. The apparatus of claim 1, wherein N is a positive even number.

4. The apparatus of claim 1, wherein N is two.

5. The apparatus of claim 1, wherein each of said N bus lines is coupled to one bit line in one of said $\log_2(N)$ pairs of bit lines via a separate transistor according to an encoding of said bus line.

6. The apparatus of claim 5, wherein each transistor has a gate coupled to one bus line, a source coupled to ground, and a drain coupled to one of said high bit line and said low bit line, according to the encoding of said bus line.

7. The apparatus of claim 1, wherein each of said N bus lines is logically NAND coupled with a clock line.

8. The apparatus of claim 6, wherein each of said drains coupled to the same bit line is logically NOR coupled together and wherein an output of said logical NOR coupling is coupled to an input of one of said $\log_2(N)$ NOR gates.

9. A system, comprising:

a processor including N bus lines, wherein N is a natural number,

$\log_2(N)$ pairs of bit lines, wherein each of said $\log_2(N)$ pairs of bit lines includes a high bit line and a low bit line, wherein each of said N bus lines is coupled to one of said high and low bit lines, $\log_2(N)$ NOR gates, each having at least a first input, a second input and an output, wherein each NOR gate is associated with one of said $\log_2(N)$ pairs of bit lines, and wherein for each NOR gate, said first input is coupled to said high bit line and said second input is coupled to said low bit line of one of said $\log_2(N)$ pairs, and a multi-hit line coupled to each output of said $\log_2(N)$ NOR gates;

at least one input-output device to couple with said processor via at least one of said N bus lines; and

at least one data storage coupled to said processor.

10. The system of claim 9, wherein N is a positive number.

11. The system of claim 9, wherein N is a positive even number.

12. The system of claim 9, wherein N is two.

13. The system of claim 9, wherein each of said N bus lines is coupled to one bit line in one of said $\log_2(N)$ pairs of bit lines via a separate transistor according to an encoding of said bus line.

14. The system of claim 13, wherein each transistor has a gate coupled to one bus line, a source coupled to ground, and a drain coupled to one of said high bit line and said low bit line, according to the encoding of said bus line.

15. The system of claim 9, wherein each of said N bus lines is logically NAND coupled with a clock line.

16. The system of claim 13, wherein each of said drains coupled to the same bit line is logically NOR coupled together and wherein an output of said logical NOR coupling is coupled to an input of one of said $\log_2(N)$ NOR gates.

17. A system, comprising:

at least one processor;

N bus lines, where N is a natural number;

$\log_2(N)$ pairs of bit lines, wherein each of said $\log_2(N)$ pairs of bit lines includes a high bit line and a low bit line, wherein each of said N bus lines is coupled to one of said high and low bit lines, $\log_2(N)$ NOR gates, each having at least a first input, a second input and an output, wherein each NOR gate is associated with one of said $\log_2(N)$ pairs of bit lines, and wherein for each NOR gate, said first input is coupled to said high bit line and said second input is coupled to said low bit line of one of said $\log_2(N)$ pairs, and a multi-hit line coupled to each output of said $\log_2(N)$ NOR gates;

at least one input-output device coupled to said at least one processor via at least one of said N bus lines; and

at least one data storage coupled to said at least one processor.

18. The system according to Claim 17, wherein said at least one processor comprises at least two processors, and wherein said at least two processors are coupled via at least one of said N bus lines.

19. The system according to Claim 17, wherein at least one of said at least one data storage is coupled to said at least one processor via at least one of said N bus lines.